REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claims 3 and 4 are cancelled.

Claims 1, 5, 12, 14, 16, 18 and 20-22 are currently being amended.

This amendment changes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 1, 5-18 and 20-22 are now pending in this application.

Claim Objections

Claims 1, 5 and 18 were objected to for informalities. In response, Applicant amends claims 1, 5 and 18 to cure the deficiencies. Accordingly, Applicant requests that the objection be withdrawn.

Claim Rejections under 35 U.S.C. § 112

Claims 1, 3-18 and 20-22 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In response, Applicant has amended the claims to remedy all antecedent basis issues. The rejection is moot in regards to cancelled claims 3 and 4. Accordingly, Applicant requests that the rejection be withdrawn.

Claim Rejections under 35 U.S.C. § 102

Claim 18 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,658,564 ("Smith"). In response, without agreeing or acquiescing to the rejection, Applicant amends claim 18 to further define the invention. In addition, Applicant respectfully traverses the rejection for the reasons set forth below.

Applicant relies on M.P.E.P. § 2131, entitled "Anticipation – Application of 35 U.S.C. § 102(a), (b) and (e)" which states, "a claim is anticipated only if each and every element set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Applicant respectfully submits that Smith does not describe each and every element of the claims.

Claim 18 is directed to a program generation method for an electronic computer executing an application program divided into a plurality of processing units, wherein said electronic computer includes a processing device with reconfigurable hardware that can create a logic circuit for each of said processing units and a control device, comprising: analyzing a control flow; implementing a command sequence procedure in which a command sequence is generated by translating the command sequence intermediate code into a form that can be executed by the electronic computer, wherein the command sequence procedure sets a time period for loading configuration data of the reconfigurable hardware or making the configuration data valid; and generating program data in which operational content of a processing unit is translated into a form that can be executed by the electronic computer, wherein the application program is divided so that each processing unit can be stored in a program data memory that holds a program creating a logic circuit for each processing unit in said reconfigurable hardware when the control flow of the application program is analyzed and divided into processing units in said analyzing a control flow step.

Accordingly, in the claimed method, configuration data of an application is divided into a size below the size of reconfigurable hardware in the system. The system is operated by "switching" (replacing) the configuration data upon execution. This sequence of the switching corresponds to the command sequence. Further, since the configuration of

reconfigurable hardware is formed from configuration data memory comprised of a plurality of banks and their selector, it is possible to preload configuration data predetermined to execute during the operation of the reconfigurable hardware. The "command sequence" includes such a load sequence of configuration data taking account of such a re-configurable hardware.

Further, the "command sequence implementation procedure" is more than just a "compile method of software/hardware," as the Examiner asserts. As recited in claim 18, a command sequence implementation procedure is the instruction sequence that sets a time for loading configuration data of reconfigurable hardware or a time for making the configuration data valid.

In contrast, Smith does not disclose, teach or suggest each and every element recited in independent claim 18. Smith discloses a reconfigurable computer system. Smith discloses partitioning an application into blocks. *See* Col. 2, lines 4-8. Smith discloses that a partitioner automatically partitions a specification written in the system design language into software and hardware functions. *See* Col. 2, lines 24-26. However, Smith fails to disclose that the command sequence implementation procedure that "sets a time period for loading configuration data of the reconfigurable hardware or making the configuration data valid," as claimed in amended independent claim 18.

M.P.E.P. § 2131 states that"[t]he identical invention must be shown in as complete detail as is contained in the...claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *See In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Here, Smith fails to disclose each and every limitation in as complete detail as is contained in independent claim 18.

Accordingly, Applicant respectfully requests that the rejection be withdrawn and claim 18 be allowed. If this rejection of the claims is maintained, the examiner is respectfully requested to point out where the above-mentioned features are disclosed in Smith.

Claim Rejections under 35 U.S.C. § 103

Claims 1, 3-5, 15-17 and 21-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,326,806 ("Smith") in view of U.S. Patent No. 6,288,566 ("Hanrahan").

Applicant relies on MPEP § 2143, which requires that all the claim limitations be considered. Considering all the claim limitations as required by MPEP § 2143.03, the cited references do not identically disclose, teach or suggest all the claim limitations. *See In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Claims 1 and 12 are directed to an electronic computer having a program for dividing an application into a plurality of processing units and generating program data and command code sequences. Claims 14 and 16 are directed to a control method for an electronic computer. Claims 20 and 21 are directed to a computer program product for an electronic computer which when executed performs a method implemented using reconfigurable hardware.

Specifically, the above claims require a method and a processing device including a program for dividing an application into a plurality of processing units and generating program data and command code sequences executed by said electronic computer, said electronic computer comprising a processing device and a control device. The program executes a command sequence implementation procedure for translating command sequence intermediate code into a data string that can be executed by the control device; said command sequence implementation procedure setting a time period for loading program data of the processing device or making the program data valid.

In sum, the claimed invention divides an application program into processing units and creates a logical circuit for every processing unit in reconfigurable hardware to improve processing speed at low cost. Further, the "command sequence implementation procedure" is more than just a "compile method of software/hardware," as the Examiner asserts. As recited in claim 1, 12, 14, 16, 20 and 21, a command sequence implementation procedure is the

instruction sequence that sets a time for loading configuration data of reconfigurable hardware or a time for making the configuration data valid.

Fallside and Smith do not disclose, teach or suggest each and every element of independent claims 1, 12, 14, 16, 18, 20 and 21. Fallside is directed to a FPGA-Based system. While Fallside teaches a control circuit for reconfiguring a FPGA in response to a predetermined condition, Fallside does not disclose, teach or suggest a method and a processing device having a program for dividing an application into a plurality of processing units and generating program data and command code sequences executed by said electronic computer, said computer comprising a processing device and a control device, wherein the program executes a command sequence implementation procedure for translating command sequence intermediate code into a data string that can be executed by the control device; said command sequence implementation procedure setting a time period for loading program data of the processing device or making the program data valid.

To cure the deficiencies of Fallside, the Office Action cites Smith and Hanrahan. However, as stated above, Smith fails to disclose that the command sequence implementation procedure "sets a time period for loading configuration data of the reconfigurable hardware or making the configuration data valid," as claimed. Further, Hanrahan fails to cure the deficiencies of Smith. Accordingly, Applicant respectfully request that the rejection be withdrawn and independent claims 1, 12, 14, 16, 18, 20 and 21 be allowed. Further, claims 3-11, 13, 15, 17 and 22 depend from one of independent claims 1, 12, 14, 16, 20 and 21 and should therefore be allowable for the reasons set forth above without regard to further patentable limitations cited therein.

If this rejection of the claims is maintained, the examiner is respectfully requested to point out where the above-mentioned features are disclosed in Fallside, Smith or Hanrahan.

Conclusion

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date 7/7/08

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